purposes only and that the number of amplifier cells varies depending on the desired gain and other requirements of a given application. Implementations for distributed amplifier 104 will be described further below in greater detail in connection with Figures 4A and 4B.--

REMARKS

Claims 1-25 are pending. The Examiner is thanked for the allowance of claims 1-19 and 25 and for the indication of allowability of claims 21 and 22 if rewritten in independent form. Claims 20, 23 and 24 were rejected. Applicants respectfully request reconsideration of the claims in view of the comments below.

The Specification has been amended to correct typographical errors. The Applicants submit that no new matter has been added by this amendment.

Attached hereto is a marked-up version of the changes made to the Specification by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made."

Claims Rejections 35 U.S.C. § 102

Claims 20, 23, and 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,166,635 to Shih. The rejection states that Shih in Fig. 1 discloses the claimed differential amplifier in the first gain stage 11 and the claimed first and second differential output amplifiers in differential amplifiers 42 and 44. Specifically, the rejection states that "one of the amplifiers 42,44 of each stage 40 may be read as the first and second differential amplifiers claimed." Applicants respectfully traverse the rejection.

Shih discloses a data line driver "having a differential input and a low distortion, high current, differential output." [Shih, col. 2, lines 22-24]. In describing Fig. 1, Shih emphasizes the "fully differential" nature of the amplifier:

> "Referring now to FIG. 2, a simplified block diagram illustrates a two stage, fully differential (differential input and differential output) digital data line driver." [Shih, col. 3, lines 24-26].

Such a "fully differential" architecture implies that the phase relationship between the differential input signal IN^- and IN^+ is maintained throughout the circuit from the input to the output. That is, the signals IN^- and IN^+ remain out-of-phase with respect to each other as they are processed through the various stages all the way out to OUT^- and OUT^+, where the "+" and "-" signs signify the out-of-phase nature of the signals. While amplifiers 42,44 are single-ended, to maintain a fully differential operation, the output of one amplifier 42 in one stage 40 would be out-of-phase with respect to the output of an amplifier 44 in the other stage 40. Accordingly, no mention could be found anywhere in Shih of any of the amplifier stages that receive differential signals and generate signals that are "in phase" with respect to each other.

In contrast, claim 20 recites, in part, first and second differential output amplifiers that receive a differential signal "made up of a first signal and a second signal, ...wherein, the first differential output amplifier is configured to generate a first single-ended output signal and the second differential output amplifier is configured to generate a second single-ended output signal that is in phase with the first single-ended output signal." Shih, therefore, fails to anticipate the claimed combination in at least this one respect.

Applicants further submit that the generation of first and second single-ended output signals that are in phase is more than a mere design choice. Rather, the claimed invention provides significant advantages over the prior art. As discussed in the Specification, the claimed invention provides for the generation of "two signals that are in phase with respect to each other [ ] at nodes 203-1 and 203-2," which, when implementing a wide-band amplifier of the type described by the present invention, enables both the signal limiting and signal splitting functions to be combined into one circuit. (Specification at page 5, line 24 and page 6, line 8). Therefore, the claimed

invention provides advantages over prior art implementations, which required "a limiter amplifier that would then be followed by a divider (or splitter) distributed amplifier. (Specification at page 5, line 24).

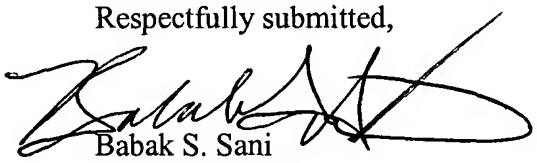
Accordingly, Applicants respectfully submit that Shih neither anticipates nor suggests the combination as set forth in claim 20. Claims 23 and 24 depend from claim 20 and thus derive patentability therefrom. Withdrawal of this rejection is therefore respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Paragraph 3 beginning at page 1, line 20 has been amended as follows:

Recent advances in optical and semiconductor processing technologies are enabling 40 Gb/s systems to move from research laboratories to production ready systems that can be manufactured in large volumes. However, the design of various functional blocks, especially at the interface with the fiber, remains a challenging task. For example, one of the most critical circuits in an optical transmitter is the amplifier in the optical modulator that drives the fiber. At the 40 Gb/s rate, the amplifier must exhibit very large bandwidth. It is also required to drive a relatively large signal (e.g., ≥ 7Vpp) **[– or is it 2.5Vpp?) signal]**. The large bandwidth requires smaller and faster transistors while the higher voltage operation requires the opposite. The driver amplifier is also required to perform a limiting function to achieve a stable eye diagram at its output. These various and competing requirements create a set of tradeoffs that make the task of designing the amplifier a particularly difficult one.

Paragraph 4, beginning at page 2, line 4 has been amended as follows:

Current approaches to designing the driver amplifier are based on a distributed amplifier architecture. This type of an **[amplifiery]** amplifier connects a number of parallel amplifier cells that are typically made up of a single transistor or a cascoded pair of transistors. The limiting function is achieved by making the amplifier **[working]** work in deep saturation. The power compression in this design, however, causes about 3-4 dB of gain loss, requiring more cells to achieve the desired overall gain or several cascaded devices. A larger number of amplifier cells, however, results in lower bandwidth and increased power consumption. An alternative approach separates the limiting function from the amplifier by using a limiter circuit that drives one or more

distributed amplifiers such that the amplifier need not operate in saturation region. There are drawbacks to this approach as well. At 40 Gb/s, most of the circuitry is implemented in a single-ended architecture and as such, the addition of a single-ended limiter reduces the overall achievable gain, while the power levels remain as another constraint.

Paragraph 18 beginning at page 5, line 11 has been amended as follows:

A simplified block diagram of a wideband amplifier 100 according to one embodiment of the invention is shown in Figure 1. Amplifier 100 includes a preamplifier 102 that receives a differential input signal Vin at its inputs IN1 and IN2. Preamplifier 102 acts as a limiter as well as a divider to produce a pair of limited output signals Vo1 and Vo2 that are in phase with respect to each other. Signals Vo1 and Vo2 are respectively applied to two input gate lines 106 and 108 of a combiner distributed amplifier 104. The output OUT of combiner distributed amplifier 104 provides the final output of amplifier 100. Distributed amplifier 104 is shown as having five amplifier cells 110 in each of its halves. It is to be understood, however, that this is for illustrative purposes only and that the number of amplifier cells varies depending on the desired gain and other requirements of a given application. Implementations for distributed amplifier 104 will be described further below in greater detail in connection with Figures 4A and 4B.